REMARKS

In the Office Action, the Examiner noted that claims 1-20 are pending in the application and that claims 1-20 are rejected. By this response, claims 1, 11, 14, and 17 are amended. In view of the above amendments and the following discussion, the Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-8 and 10-20 as being anticipated by Chen (United States patent 6,687,888, issued February 3, 2004). More specifically, the Examiner stated that Chen teaches designing an integrated circuit (IC) in accordance with timing constraint data, identifying first and second sets of logic paths, and selectively optimizing the IC to reduce power consumption in response to the first and second logic paths. (Office Action, p. 2-3). The rejection is respectfully traversed.

Chen generally teaches optimizing an IC for both power consumption and speed. (See Chen, Abstract). In particular, Chen teaches a global optimization technique where a design is optimized for both timing and power simultaneously. In one example, Chen employs a genetic optimization technique (Chen, col. 8, line 30-67; FIG. 3A; see also col. 9, lines 1-62; FIG. 4). If any path exceeds timing constraints, a score for an individual in a population is negatively affected. The score is affected inversely to power dissipation. (Chen, col. 8, lines 48-57). An updated netlist (design result) is produced at the end of the process. In another example, a genetic optimization technique is combined with a greedy optimization technique. (Chen, col. 11, line 32 to col. 12, line 19; FIG. 6). In all examples disclosed in Chen, timing and power are optimized simultaneously to produce an optimized design result.

In view of the foregoing, Chen does not teach each and every element of Applicants' invention recited in claim 1. Namely, Chen does not teach or suggest "designing the integrated circuit in accordance with timing constraint data to produce a design result" and then "selectively optimizing the integrated circuit to reduce power

consumption...." (Applicants' claim 1). In the interests of furthering prosecution and further clarification, Applicants have amended claim 1 to indicate that a design result is produced from designing the integrated circuit in accordance with timing constraint data. The design result is a complete result optimized for timing only. (supported by Applicants' specification, ¶0016; FIG. 2). Thus, in Applicants' claim 1, an integrated circuit is first designed in conformity with timing constraint data to produce a design result (e.g., a timing-driven process) and then optimized to reduce power consumption (e.g., a power-driven process).

In contrast, Chen teaches a single global optimization process, where the design is simultaneously optimized for both timing and power. A design result optimized for timing, but not for power, is not produced in Chen. Moreover, Chen does not teach or suggest optimizing a design for timing to produce a result, and then optimizing the design for power. In Chen, any power optimizations are part of the general optimization process for timing and power. Once the circuit design conforms to the general optimization (e.g., the genetic optimization or greedy optimization) and an optimized design result is produced, no further power optimizations are performed.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Chen does not teach designing the integrated circuit in accordance with timing constraint data to produce a design result and then selectively optimizing the integrated circuit to reduce power consumption, Chen does not teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Chen does not anticipate Applicant's invention recited in claim 1.

Claim 11 recites, among other features, a computer readable medium for designing the integrated circuit in accordance with timing constraint data to produce a design result and selectively optimizing the integrated circuit to reduce power consumption. Claim 14 recites, among other features, a means for designing the integrated circuit in accordance with timing constraint data to produce a design result and a means for selectively optimizing the integrated circuit to reduce power consumption. Claim 17 recites, among other features, designing the integrated circuit

in accordance with timing constraint data to produce a design result and selectively optimizing the integrated circuit to reduce power consumption. Each of these features are similar to those of claim 1 emphasized above. For the same reasons discussed above, Chen does not teach each and every element of Applicants' claims 11, 14, and 17.

Finally, claims 2, 4, 6-8, and 12-13, 15-16, and 18-20 depend, either directly or indirectly, from claims 1, 11, 14, and 17 and recite additional features therefor. Since Chen does not anticipate Applicants' invention as recited in claims 1, 11, 14, and 17, dependent claims 2, 4, 6-8, and 12-13, 15-16, and 18-20 are also not anticipated and are allowable. In view of the foregoing, Applicants contend that claims 1-2, 4, 6-8, and 11-20, are not anticipated by Chen and, as such, fully satisfy the requirements of 35 U.S.C. §102. Accordingly, Applicants respectfully request that the rejection to such claims be withdrawn.

II. Rejection Of Claims Under 35 U.S.C. §103

The Examiner rejected claim 9 as being unpatentable over Chen in view of Dave (United States patent 6,178,542, issued January 23, 2001). The rejection is respectfully traversed.

More specifically, the Examiner noted that Chen does not disclose the feature of the IC having a plurality of logic paths, where the threshold is defined by a percentage of a parameter in the timing constraint data. (Office Action, p. 5). The Examiner stated that Dave teaches such a threshold. (Office Action, p. 5). The Examiner concluded that it would have been obvious to combine Dave with Chen to arrive at Applicants' invention of claim 9. Applicants respectfully disagree.

Dave generally teaches hardware-software co-synthesis of embedded system architectures using quality of architecture metrics. (See Dave, Abstract). Dave, however, does not teach or suggest designing the integrated circuit in accordance with timing constraint data to produce a design result and then selectively optimizing the integrated circuit to reduce power consumption. Chen also fails to teach such a feature, as discussed above. Since neither Chen nor Dave teach such a feature, no conceivable combination of Chen and Dave render obvious Applicants' invention of

claim 1. Therefore, Applicants contend that the invention of claim 9 is patentable over the combination of Chen and Dave and, as such, fully satisfies the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the rejection of claim 9 be withdrawn.

CONCLUSION

Thus, Applicant submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Kim Kanzaki, Ph.D.
Attorney for Applicants
Reg. No. 37,652

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 29, 2006.

Pat Tompkins — Pat Tompkins
Name *Signature*